ABSTRACT OF THE DISCLOSURE

Interconnections are formed over an interlayer insulating film which covers MISFETQ1 formed on the principal surface of a semiconductor substrate, while dummy interconnections are disposed in a region spaced from such interconnections. Dummy interconnections are disposed also in a scribing area. Dummy interconnections are not formed at the peripheries of a bonding pad and a marker. In addition, a gate electrode of a MISFET and a dummy gate interconnection formed of the same layer are disposed. Furthermore, dummy regions are disposed in a shallow trench element-isolation region. After such dummy members are disposed, an insulating film is planarized by the CMP method.